National Institute of Electronics and Information Technology (NIELIT)
Dwarka, New Delhi
राष्ट्रीय इलेक्ट्रॉनिकी एवं सूचना प्रौद्योगिकी संस्थान, द्वारका, नई दिल्ली -110077

DETAILED ADVERTISEMENT
(Advt. No. NHQ**--2025/22/12**NC ((**3160304)**

NIELIT requires the following person purely on contract basis on consolidated remuneration initially for a period of one year: -

1.Assistant Professor					
Branch/ University Campus	**Electronics and Communication Engineering and Allied branches**	**Electrical Engineering and Allied Branches**	**Computer Science Engineering and Allied Branches**	**Applied Science**	**Humanities**
Position Code	**2507-ASPECE**	**2507-ASPEE**	**2507-ASPCSE**	**2507-ASPAS**	**2507-ASPHU**
NDU-Roper	2	-	2	-	-
NIELIT-Aizawl	1	-	2	-	-
NIELIT-Agartal		-	1	-	-
NIELIT-Aurangabad	1	-	3	-	-
NIELIT-Gorakhpur	1	1	2	2	1
NIELIT-Imphal	-	-	1	-	-
NIELIT-Itanagar	-	-	1	-	-
NIELIT- Kekri (Ajmer)	-	-	2	-	-
NIELIT-Kohima	-	-	1	-	-
NIELIT-Patna	-	-	2	-	-
NIELIT-Srinagar	-	-	1	-	-
NIELIT-Calicut	1	-	-	-	-
Tenure/ Period		1 year (purely on contract basis)			
Age Limit		Up to 50 Years (as on last date of application)			
Emoluments (Monthly) (inclusive of statutory compliances, if any) [CTC		Rs. 60,000/- to Rs. 70,000/- P.M			

QUALIFICATION FOR APPOINTMENT OF TEACHING FACULTY: ASSISTANT PROFESSOR- ELECTRONICS AND COMMUNICATION ENGINEERING AND ALLIED BRANCHES / ELECTRICAL ENGINEERING AND ALLIED BRANCHES/ COMPUTER SCIENCE ENGINEERING AND ALLIED BRANCHES

B. E. / B. Tech. and M. E. / M. Tech. or Integrated M. Tech. in relevant branch with first class or equivalent in any one of the degrees.
'OR'
1st class of equivalent in B.E./ B. Tech in relevant branch with Ph.D in relevant branch from a recognized university.

For Humanities and Applied Sciences
A Master's degree with 55% marks (or an equivalent grade in a point-scale wherever the grading system is followed) in a concerned/relevant/allied subject from an Indian University, or an equivalent degree from an accredited foreign university

Besides fulfilling the above qualifications, the candidate must have cleared the National Eligibility Test (NET) conducted by the UGC or the CSIR, or a similar test accredited by the UGC, like SLET/SET or who are or have been awarded a Ph. D. Degree in accordance with the University Grants Commission (Minimum Standards and Procedure for Award of M.Phil./Ph.D. Degree) Regulations, 2009 or 2016 and their amendments from time to time as the case may be exempted from NET/SLET/SET :

Provided, the candidates registered for the Ph.D. programme prior to July 11, 2009, shall be governed by the provisions of the then existing Ordinances/Bye-laws/Regulations of the Institution awarding the degree and such Ph.D. candidates shall be exempted from the requirement of NET/SLET/SET for recruitment and appointment of Assistant Professor or equivalent positions in Universities/Colleges/Institutions subject to the fulfillment of the following conditions :-
a) The Ph.D. degree of the candidate has been awarded in a regular mode;
b) The Ph.D. thesis has been evaluated by at least two external examiners;
c) An open Ph.D. viva voce of the candidate has been conducted;
d) The Candidate has published two research papers from his/her Ph.D. work, out of which at least one is in a refereed journal;
e) The candidate has presented at least two papers based on his/her Ph.D work in conferences/seminars sponsored/funded/supported by the UGC / ICSSR/ CSIR or any similar agency.

2. Associate Professor				
Branch/ University Campus	**Electronics and Communication Engineering and Allied branches**	**Computer Science Engineering and Allied Branches**	**Applied Science**	**Humanities**
Position Code	**2507-APECE**	**2507-APCSE**	**2507-APAS**	**2507-APHU**
NIELIT-Aizawl	1	-	-	-
NIELIT-Agartal	-	-	-	-
NIELIT-Aurangabad	1	1	1 (Physics)	1 (English)
NIELIT-Gorakhpur	1	1	-	-
NIELIT- Kekri (Ajmer)	-	1	-	-
NIELIT-Patna	-	1	-	-
NIELIT-Srinagar	2	2	-	-
Tenure/ Period	1 year (purely on contract basis)			
Age Limit	Up to 50 Years (as on last date of application)			
Emoluments (Monthly) (inclusive of statutory compliances, if any) [CTC]	Rs. 80,000/- to Rs. 90,000/- P.M			

QUALIFICATION FOR APPOINTMENT OF TEACHING FACULTY: ASSOCIATE PROFESSOR- ELECTRONICS AND COMMUNICATION ENGINEERING AND ALLIED BRANCHES / COMPUTER SCIENCE ENGINEERING AND ALLIED BRANCHES

B.E./B.Tech and M.E./ M.Tech in relevant branch with 1st class or equivalent either in B.E./B.Tech or M.E./ M.Tech from a recognized University.

'OR'

1st class or equivalent in B.E./B.Tech in relevant branch / 1st class in MCA and Ph.D. in relevant branch from a recognized University.

Qualifications as above with Ph.D. or equivalent, in relevant branch.

At least total 6 research publications in SCI journals/UGC-CARE listed/AICTE approved list journals.

Experience: - A minimum of 6 years of experience of teaching and/or research in an academic/research position equivalent to that of Assistant Professor in a University/College/accredited research institution /industry out of which at least 2 years shall be post Ph.D. experience.
In case of research experience, good academic record and books/research paper publications/IPR/patents record shall be required as deemed fit by the expert members of the Selection Committee.

If the experience in industry is considered, the same shall be at managerial level equivalent to Assistant Professor with active participation record in devising/designing, planning, executing, analysing, quality control, innovating, training, technical books/research paper publications/ IPR/patents etc., as deemed fit by the expert members of the Selection Committee.

For Humanities and Applied Sciences
i) A good academic record, with a Ph.D. Degree in the concerned/allied/relevant disciplines.
ii) A Master's Degree with at least 55% marks (or an equivalent grade in a point-scale, wherever the grading system is followed).
iii) A minimum of eight years of experience of teaching and / or research in an academic/research position equivalent to that of Assistant Professor in a University, College or Accredited Research Institution/industry with a minimum of seven publications in the peer-reviewed or UGC-listed journals

3. Professor		
Branch/ University Campus	**Electronics and Communication Engineering and Allied branches**	**Computer Science Engineering and Allied Branches**
Position Code	**2507-PRECE**	**2507-PRCSE**
NIELIT-Aizawl	1	-
NIELIT-Aurangabad	-	1
NIELIT-Gorakhpur	1	-
NIELIT- Kekri (Ajmer)	-	1
NIELIT-Srinagar	1	1
Tenure/ Period	1 year (purely on contract basis)	
Age Limit	Up to 50 Years (as on last date of application)	
Emoluments (Monthly) (inclusive of statutory compliances, if any) [CTC]	Rs. 90,000/- to Rs. 1,00,000/- P.M	

QUALIFICATION FOR APPOINTMENT OF TEACHING FACULTY: PROFESSOR- ELECTRONICS AND COMMUNICATION ENGINEERING AND ALLIED BRANCHES / COMPUTER SCIENCE ENGINEERING AND ALLIED BRANCHES

B.E./B.Tech and M.E./M.Tech in relevant branch with 1st class or equivalent either in B.E./B.Tech or M.E./M.Tech from a recognized University.

'OR'

1st Class or equivalent in B.E./B.Tech in relevant branch and Ph.D in relevant branch from a recognized University.

Qualifications as above with PhD or equivalent, in the relevant branch.

At least total 6 research publications at the level of Associate Professor in SCI journals/UGC-CARE listed/AICTE approved list journals and at least 2 successful Ph.D. guided as Supervisor/Co-supervisor.

'OR'

At least 10 research publications at the level of Assistant Professor/Associate Professor in SCI journals/UGC-CARE listed/AICTE approved list journals.

Experience: - A minimum of 10 years of experience of teaching/ research/industry out of which at least 3 years shall be at the post equivalent to that of an Associate Professor.

In case of research experience, good academic record and books/research paper publications/IPR/patents record shall be required as deemed fit by the expert members of the Selection Committee.

If the experience in industry is considered, the same shall be at managerial level equivalent to Associate Professor with active participation record in devising/designing, planning, executing, analysing, quality control, innovating, training, technical books/research paper publications/ IPR/patents etc., as deemed fit by the expert members of the Selection Committee

4. Name of the Position	**Team Lead (VLSI Design)**
Position Code	**2507-TLVD**
No. of Position & Location	05 (Five) for NIELIT Dwarka office /NIELIT Kidwai Nagar office /NIELIT CoE Noida or any office of NIELIT in Noida or Delhi
Tenure/ Period	1 year (purely on contract basis)
Age Limit	Up to 50 Years
Emoluments (Monthly) (inclusive of statutory compliances, if any) [CTC]	Rs. 95,000/- P. M.
Eligibility Criteria and Experience	**Essential: -** Bachelor's/Master's/PhD in Electronics & Communication Engineering, VLSI Design, or related field. **Experience:** 4 years of relevant experience in industry/academia/R&D Organization **Note:** Duration of PhD will be counted as R&D experience **Job description:** Key responsibilities include: • Lead the design and development of reusable IP blocks using open-source EDA tools, and oversee their validation and documentation • Drive end-to-end ASIC/SoC design workflows using open-source EDA tools, and coordinate benchmarking of developed IPs and ASICs/SoCs against results from

	closed-source EDA tools to ensure performance, area, and power metrics are industry-comparable • Lead a cross-functional team for content creation, tool integration, and platform delivery. • Design and develop audio-visual content and labs for RTL-to-GDSII flow using open-source EDA tools. • Oversee integration of open source EDA tools and design flows into the web-based EdTech platform. • Collaborate with academic and industry experts to develop and update modular, job-ready curricula. • Mentor junior engineers and trainers; drive knowledge sharing and skill development. • Facilitate community-building, including forums, bootcamps, and mentorship initiatives. • Ensure quality, track learner feedback, and implement continuous improvements in training and platform features. **Preferred Skills** • Strong understanding of instructional design principles and curriculum frameworks (AICTE, NEP, etc.). • Familiarity with LMS platforms (e.g., Moodle, Canvas) and digital content formats (SCORM, MP4, PDFs). • Experience working with academic institutions or government skilling programs. • Excellent organizational, communication, and mentoring skills.
5. Name of the Position	**VLSI Design Expert/ Junior VLSI Engineer**
Position Code	**2507-VLSIDE**
No. of Position & Location	**10 (Ten)** for NIELIT Dwarka office /NIELIT Kidwai Nagar office /NIELIT CoE Noida or any office of NIELIT in Noida or Delhi
Tenure/ Period	1 year (purely on contract basis)
Age Limit	Up to 45 Years
Emoluments (Monthly) (inclusive of statutory compliances, if any) [CTC]	Rs. 40,000/- P.M
Eligibility Criteria and Experience	**Essential: -** Master's/PhD in Electronics & Communication, Electrical Engineering, VLSI Design, or related field. OR Bachelor in Electronics & Communication, Electrical Engineering, VLSI Design, or related field with one year experience **Job description:** Key responsibilities include: • To assist in design and development of reusable IP

	blocks using open-source EDA tools, their validation and documentation • Design and develop in-depth academic and practical content in one or more of the following domains: o **RTL Design & Integration** o **Physical Design** o **Synthesis and STA** o **DFT and ATPG** o **Analog and Mixed-Signal Design** o **Digital and Analog Design Verification** o **Standard Cell and PDK-based design** • Create reproducible design labs and projects using open-source tools such as: o **Magic**, **KLayout**, **Yosys**, **OpenROAD**, **Ngspice**, **Xschem**, **Netgen**, **GHDL**, **Verilator**, etc. • Develop and document exercises, assignments, and mini-projects for each design domain. • Record demos or work with AV teams to create training videos and tutorials. • Collaborate with content designers, platform developers, and trainers to align content with platform capabilities. • Test and validate open-source flows with actual design examples and student-level reproducibility. • Mentor junior engineers, interns, and trainers when needed. **Preferred Skills** • Prior teaching, curriculum development, or instructional design experience. • Exposure to cloud-based VLSI design environments or FPGA-based learning kits. • Knowledge of modern teaching aids – LMS platforms (e.g., Moodle), video content creation, screen recording tools. • Strong written and verbal communication skills.
6. Name of the Position	**Senior Trainers (VLSI Design)/ Senior VLSI Engineer**
Position Code	**2507-STVD**
No. of Position & Location	**4 (Four),** for NIELIT Dwarka office /NIELIT Kidwai Nagar office /NIELIT CoE Noida or any office of NIELIT in Noida or Delhi
Tenure/ Period	1 year (purely on contract basis)
Age Limit	Up to 50 Years
Emoluments (Monthly) (inclusive of statutory compliances, if any) [CTC]	Rs. 65000/- P.M
Eligibility Criteria and Experience	**Essential:** B.Tech/M.Tech in ECE, EE, VLSI Design or related field.

	Experience: 3 years of relevant experience in industry/ academia/ R&D Organization **Note:** Duration of PhD will be counted as R&D experience **Job description:** • To assist in design and development of reusable IP blocks using open-source EDA tools, their validation and documentation • To develop end-to-end ASIC/SoC design workflows using open-source EDA tools, and coordinate benchmarking of developed IPs and ASICs/SoCs against results from closed-source EDA tools to ensure performance, area, and power metrics are industry-comparable • Conduct Train-the-Trainer (ToT) programs for faculty and academic partners. • Deliver workshops, bootcamps, and webinars for students, faculty, and professionals. • Use open-source tools (e.g., Yosys, Magic, OpenROAD, KLayout, Ngspice, Verilator, Xschem) to conduct hands-on sessions. • Help participants with design challenges, practical labs, and capstone projects. • Serve as a point of contact for 10–20 assigned academic institutions. • Guide partner faculty in adopting and integrating course content into their curricula. • Provide ongoing academic mentorship and resolve technical or pedagogical queries. • Ensure learning continuity via LMS, forums, or online sessions. • Collect feedback, performance data, and learning outcomes. • Work with the central content and platform team to suggest improvements. • Assist in conducting assessments, certifications, and project evaluations. • Help users onboard and use the open-source chip design platform effectively. • Report technical issues and contribute to documentation and FAQs. • Maintain a knowledge base and support structure for learners and faculty.
7. Name of the Position	**Team Leader (Platform Development Team)**
Position Code	**2507-TLPDT**
No. of Position & Location	**1 (One),** for NIELIT Dwarka office /NIELIT Kidwai Nagar office /NIELIT CoE Noida or any office of NIELIT in Noida or Delhi

Tenure/ Period	1 year (purely on contract basis)
Age Limit	Up to 45 Years
Emoluments (Monthly) (inclusive of statutory compliances, if any) [CTC]	Rs. 95,000/- P.M
Eligibility Criteria and Experience	**Essential: -** • Bachelor's degree in Computer Science, IT, or related field (or equivalent experience). **Experience:** • 5 years of experience **Job description:** Key responsibilities include: • Develop and maintain scalable web applications using Java, Spring Boot, and React for EdTech Platform of NIELIT • Lead a small team of developers for continuous update of platform and add new features as per requirement of platform • Design and implement RESTful APIs and integrate them with the frontend • Use Monaco Editor to support advanced code-editing features on the platform • Manage frontend components with React Bootstrap • Package and manage backend services using Maven • Work with DevOps to ensure CI/CD and containerization best practices • Write unit and integration tests to ensure code quality • Perform code reviews and maintain high coding standards • Debug production issues and ensure platform uptime and performance **Preferred Skills** - Strong proficiency in Java and Spring Boot - Strong command over React and modern JavaScript/TypeScript - Experience with Monaco Editor integration in React apps - Familiarity with Maven, REST APIs, Git, and CI/CD pipelines - Understanding of microservices architecture and containerized deployments (Docker/Kubernetes) - Experience working with cloud services on AWS - Familiarity with educational tech platforms or LMSs - Prior experience with Kubernetes or DevOps pipelines
8. Name of the Position	**DevOps Engineer**
Position Code	**2507-DOE**
No. of Position & Location	**4,** for NIELIT Dwarka office /NIELIT Kidwai Nagar office /NIELIT CoE Noida or any office of NIELIT in Noida or Delhi

Tenure/ Period	1 year (purely on contract basis)
Age Limit	Up to 40 Years
Emoluments (Monthly) (inclusive of statutory compliances, if any) [CTC]	Rs. 65,000/- P.M
Eligibility Criteria and Experience	**Essential: -** Bachelor's degree in Computer Science, IT, or related field (or equivalent experience). **Experience:** 1 years of experience with cloud platforms and virtualization technologies. AWS experience is desired. **Job description:** Key responsibilities include: • Manage Kubernetes-based infrastructure on AWS EKS • Manage CI/CD pipelines for automated testing, building, and deployment • Ensure high availability, reliability, and performance of services on production • Implement monitoring, logging, and alerting using tools like Prometheus, Grafana, ELK stack, or CloudWatch • Manage secrets, certificates, and access controls securely • Define and maintain infrastructure as code using Terraform or AWS CloudFormation • Optimize deployment processes, cost, and scalability across environmentsManage user authentication, data security, and access control mechanisms. • Set up storage solutions for lab files, simulation data, and course materials. • Collaborate with platform developers, instructional teams, and VLSI engineers to ensure infrastructure readiness. **Preferred Skills** • Expertise in Kubernetes (EKS) cluster management and container orchestration • Strong knowledge of AWS services (EKS, EC2, RDS, S3, IAM, CloudWatch, etc.) • Proficiency in scripting (Bash, Python, or similar) • Experience with CI/CD tools (GitHub Actions, Jenkins, or similar) • Knowledge of Docker, Helm, and infrastructure monitoring tools • Experience implementing security best practices (firewalls, IAM roles, VPC setups) Strong problem-solving and analytical skills. • Excellent communication and team collaboration abilities.
9. Name of the Position	**Full Stack Engineer**

Position Code	**2507-FSE**
No. of Position & Location	**6 (Six),** for NIELIT Dwarka office /NIELIT Kidwai Nagar office /NIELIT CoE Noida or any office of NIELIT in Noida or Delhi
Tenure/ Period	1 year (purely on contract basis)
Age Limit	Up to 45 Years
Emoluments (Monthly) (inclusive of statutory compliances, if any) [CTC]	Rs. 65,000/- P.M
Eligibility Criteria and Experience	**Essential: -** Bachelor's degree in Computer Science, IT, or related field (or equivalent experience). **Experience:** 1 years of experience with full stack development **Job description:** Key responsibilities include: - Develop and maintain scalable web applications using Java, Spring Boot, and React - Design and implement RESTful APIs and integrate them with the frontend - Use Monaco Editor to support advanced code-editing features on the platform - Manage frontend components with React Bootstrap - Package and manage backend services using Maven - Work with DevOps to ensure CI/CD and containerization best practices - Write unit and integration tests to ensure code quality - Perform code reviews and maintain high coding standards - Debug production issues and ensure platform uptime and performance **Preferred Skills** - Strong proficiency in Java and Spring Boot - Strong command over React and modern JavaScript/TypeScript - Experience with Monaco Editor integration in React apps - Familiarity with Maven, REST APIs, Git, and CI/CD pipelines - -Understanding of microservices architecture and containerized deployments (Docker/Kubernetes) - - Experience working with cloud services on AWS
10. Name of the Position	**Graphics Designer**
Position Code	**2507-GD**
No. of Position & Location	**1 (One),** for NIELIT Dwarka office /NIELIT Kidwai Nagar office /NIELIT CoE Noida or any office of NIELIT in Noida or Delhi
Tenure/ Period	1 year (purely on contract basis)
Age Limit	Up to 45 Years

Emoluments (Monthly) (inclusive of statutory compliances, if any) [CTC]	Rs. 40000/- P.M
Eligibility Criteria and Experience	**Essential:** Bachelor's Degree in Graphic Design, Multimedia Arts, Computer Science or a related field **Experience:** 1 years of experience in graphics design of educational content **Job description:** • Create and design digital assets including social media graphics, website banners, brochures, presentations, and print materials. • Edit and produce high-quality videos for social media, marketing campaigns, training modules, and promotional content. • Collaborate with content, marketing, and product teams to bring concepts to life through compelling visuals and motion. • Ensure brand consistency across all visual content. • Stay up-to-date with the latest design and video trends, techniques, and tools. • Manage multiple design and video projects with strong attention to detail and adherence to deadlines. **Preferred Skill:** • Proven experience as a graphic designer and video editor. • Proficient in Adobe Creative Suite (Photoshop, Illustrator, InDesign, Premiere Pro, After Effects) • Proficient in Canvas Design tools • Understanding of color theory, typography, composition, and motion graphics.
11. Name of the Position	**Sr. Resource Person**
Position Code	**2507-SRP**
No. of Position & Location	**1 (One),** for NIELIT Dwarka office /NIELIT Kidwai Nagar office /NIELIT CoE Noida or any office of NIELIT in Noida or Delhi
Tenure/ Period	1 year (purely on contract basis)
Age Limit	Up to 50 Years
Emoluments (Monthly) (inclusive of statutory compliances, if any) [CTC]	Rs. 60000/- P.M
Eligibility Criteria and Experience	**Essential: -** Graduate in any discipline (preferably in Science, Engineering, or Management). **Experience:** Minimum 4 Years of experience in administrative/coordination roles specially in handling government project **Job Description:**

	• Assist the Program Head in day-to-day coordination of training, meetings, and project activities. • Maintain project documentation, reports, meeting minutes, and progress trackers. • Communicate with faculty coordinators, trainers, and institutional representatives as directed. • Follow up on tasks assigned to different teams and prepare brief status updates. • Help organize webinars, workshops, and outreach events by handling logistics and communication. • Support data entry and management of training records, feedback forms, and attendance. • Handle basic correspondence and email communications. • Ensure smooth internal coordination among content teams, platform developers, and trainers.
12. Name of the Position	**Consultant (Design Verification & EDA Integration)**
Position Code	**2507-CONS-DVEDAI**
No. of Position & Location	**1 (One),** Hybrid (Remote with Minimum 8 days onsite presence per Months.
Tenure/ Period	1 year (purely on contract basis)
Age Limit	Up to 50 Years
Emoluments (Monthly) (inclusive of statutory compliances, if any) [CTC]	Rs. 2.50 Lakhs /- P.M
Eligibility Criteria and Experience	• B.E./B.Tech/M.Tech in Electronics, VLSI, or related fields • Minimum 8 years of experience in ASIC/FPGA design verification • Strong knowledge of SystemVerilog, UVM, coverage-driven verification • Experience in open-source EDA tools and scripting (Python, TCL, Make) **Scope of Work & Deliverables:** - Development of high-quality AV content on SystemVerilog, UVM, and functional verification - Creation of reusable verification environments for IPs like UART, SPI, I2C, GPIO, RISC-V Core - Design of virtual labs using Verilator, SymbiYosys, GTKWave, etc. - Mentorship of contributors and academic partners - Support in certification and learner evaluation materials
13. Name of the Position	**Senior Resource Person (Project Officer)**
Position Code	2507-SRPPO
No. of Position	01 (One) NIELIT Corporate Office
Tenure/ Period	1 year (purely on contract basis)
Age Limit	Up to 50 Years

Emoluments (Monthly) (inclusive of statutory compliances, if any) [CTC]	Rs. 60,000/- to 80000/- P.M (Depending upon the Qualification and Experience)
Eligibility Criteria and Experience	**Essential: -** Graduation in any discipline **Experience:** 04 Years of total experience in executing and monitoring of projects. **Job Description:** Key responsibilities include: • Support to overall coordination/ management of the project activities. • Liasoning with various stakeholders/nodal agencies. • Monitoring of technical & financial progress. • Assist Stakeholders /various Committees (PRSG, AC, CMC, CC), and organizing review meetings, preparation of minutes, coordinate necessary logistics and facilitate consultations as per terms of reference. • Support Stakeholders /Committees/IAs in formulation of plans, reports, guidelines, etc. • Monitor overall implementation of project activities • To create awareness and mobilization of various stakeholders • Assist in design, development & deployment of Centralized portal. Creation and maintenance of MIS for capturing Data related to the project • Coordinating with 3rd Party for Impact Assessment. • Any other work related to the Scheme implementation.
14. Name of the Position	**Resource Person**
Position Code	2507-RP
No. of Position	01 (One) NDU, Roper
Tenure/ Period	1 year (purely on contract basis)
Age Limit	Up to 50 Years
Emoluments (Monthly) (inclusive of statutory compliances, if any) [CTC]	Rs. Rs. 67,700/- P. M. P. M.
Eligibility Criteria and Experience	**Essential: -** Master's Degree with at least 55% of the marks or an equivalent grade in a point scale wherever grading system is followed. **Experience:** At least 15 years of experience as Assistant Professor in the Academic Level 11 and above OR 8 years of service in the Academic Level 12 and above including as Associate Professor along with 3 years' experience in educational administration OR Comparable experience in research establishment and/ or other institutions of higher education OR 15 years administrative experience of which 8 years shall be as Deputy Registrar or an equivalent post

15. Name of the Position	**Consultant**
Position Code	2507-CONSUL
No. of Position	01 (One) Post at NIELIT HQ
Tenure/ Period	1 year (purely on contract basis)
Age Limit	Up to 40 Years (as on last date of application)
Emoluments (Monthly) (inclusive of statutory compliances, if any) [CTC]	Rs. 70,000/-
Eligibility Criteria and Experience	**Essential eligibility:** Bachelor's degree in technology or engineering or equivalent in the field of Computer Science / Information Technology / Cyber Security / Electronics and Communications with at least 60% marks in aggregate. OR MTech. in the field of Computer Science / Information Technology / Cyber Security / Electronics and Communications / MCA / NIELIT 'B' Level Degree, with at least 60% marks in aggregate. **Post Qualification Experience (after acquiring essential qualification:** At least Five (05) Year post qualification experience in conduction of Large/Enterprise Level Online Examinations including managing of data & support to Exam Centers in configuration and troubleshooting/resolving issues. **Desired Knowledge / Qualification / Certification:** • Working Knowledge/Expertise of SQL Server. • Knowledge of IIS, LAN Configuration, Server Management. • Working Knowledge/Expertise of MS Office. • Good analytical and problem-solving approach. • Strong User-interaction skill and co ordination skill Ability to remain calm and focused under extremely stressful situations Ability to work in shifts. • Work experience of Support/Incident management is desirable. • He/She should have at least 3 years of experience in managing the complete examination process of large-scale IT/ICT/e Governance projects.

General Terms & Conditions:

1. The qualification of candidates must be from Govt. University or Govt. recognized University/ Institutions.
2. Applicants with last semester result awaited or incomplete degrees are not eligible to apply.
3. Cut-off date for calculating age and experience shall be last date of receipt of applications i.e. (last date of receipt of applications).
4. Duly filled offline application with self-attested supporting should reach on or before (last date of receipt of applications) to the address: Registrar, National Institute of Electronics & Information Technology (NIELIT) NIELIT Bhawan, Plot No. 3, PSP Pocket, Institutional Area Sector-8, Dwarka, New Delhi-110077. Applications received after the due date shall be summarily rejected.
5. Non-refundable Registration Fee of Rs. 500/- per position to be deposited through online mode. The Candidates may deposit registration fee in the account of NIELIT in the given Bank account:

Name of the office	National Institute of Electronics and Information Technology, New Delhi

Bank Account Number	604820100000012
Bank Name	Bank of India
IFSC Code	BKID0006048

6. Applicants are required to fill Application Forms as per the details given below:
   A. Application Form_Faculty.pdf – to be filled for the positions of Assistant professor, Associate Professor and Professor
   B. Application Form _Consultant -Design Verification and EDA Integration.pdf – to be filled for the position of Consultant-Design Verification and EDA Integration
   C. ApplicationForm_Other.pdf – to be filled for rest of the positions
7. Applications received without requisite application fee (Rs. 500/-) shall be summarily rejected.
8. The applicants applying for the contractual position of Consultant- Design Verification and EDA Integration are required to sign an Agreement at the time of joining.
9. The applicants who are applying for the contractual position of Assistant Professor, Associate Professor and Professor are only allowed to appear in the Interview in Online/Offline mode. The applicants who appear in the Interview (after screening of document) in Online mode will be issued Offer Letter only after the clearance of Document Verification.
10. **Screening (based on the documents attached by applicant with application form) will be done before actual Document Verification and Interview**
11. **Only those candidates who clears Screening will be called for Document Verification and the candidates who clear document verification will be called for Interview.**
12. NIELIT has the right to accept or reject the application without assigning any reason thereof.
13. Applicants are advised to visit the website of NIELIT **http://nielit.gov.in/recruitments** for any updates.
14. No separate communication shall be made in any other form.
15. The number of vacancy is tentative and liable to change as per the requirement of NIELIT.
16. The Remuneration mentioned above is consolidated salary (CTC). The selected candidate will not be paid any other financial benefits like Medical, HRA, Transport etc. except the consolidated salary.
17. Selection of candidate for appointment to the above mentioned position will be based on the performance of the candidates in the interview and as found eligible as per prescribed criteria.
18. The selected candidate will be engaged purely on contract basis initially for a period of one year, which may be extended depending upon the requirement and performance of the candidate.
19. The offer of appointment for the selected candidate will be subject to verification of original certificates/testimonials at the time of interview and completeness of other formalities.
20. NIELIT will also create a panel for contractual deployment and the candidates will be selected for deployment on contract from the panel as and when required.
21. Only those candidates who deposit requisite registration fee of Rs. 500/-, clear document verification and successful interaction will be empaneled.
22. Empanelment means the shortlisted candidates will be in the panel of NIELIT for one year. They may be deployed in specific Govt. department/ NIELIT as per department requirements purely on contract basis. Mere empanelment does not ensure deployment in any department nor provide any right to candidate to claim for deployment.
23. Empaneled candidates list will valid for one year from the date of result declaration.
24. Candidates will not be entitled to claim any TA/DA for appearing in Interview.
25. Canvassing/trying to influence NIELIT employees to secure the job in any manner shall disqualify the candidate.
26. In the case of any legal dispute, the jurisdiction shall be Delhi.

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